PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of	Docket No: Q66664
Keld LANGE, et al.	
Appln. No.: 09/981,784	Group Art Unit: 2617
Confirmation No.: 6691	Examiner: Sam BHATTACHARYA
Filed: October 19, 2001	

For: BASE STATION OF A RADIO-OPERATED COMMUNICATIONS SYSTEM

REPLY BRIEF PURSUANT TO 37 C.F.R. § 41.41

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. § 41.41, Appellant respectfully submits this Reply Brief in response to the Examiner's Answer dated July 18, 2007. Entry of this Reply Brief is respectfully requested.

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STATUS OF CLAIMS

Claims 1-16 and 19-24 are all the claims pending in the application. Claims 1-16 and 19-24 are rejected under 35 U.S.C. § 103(a). The rejected claims 1-16 and 19-24 are being appealed.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

There are four issues on Appeal.

The first issue is whether claims 1, 3, 6-13, and 19 are improperly finally rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,366,606 to Sriram (hereinafter "Sriram") in view of U.S. Patent No. 6,366,607 to Ozluturk et al. (hereinafter "Ozluturk").

The second issue is whether claims 2, 14, and 16 are improperly finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Sriram in view of Ozluturk and U.S. Patent No. 4,827,499 to Warty (hereinafter "Warty").

The third issue is whether claims 4, 5, and 15 are improperly finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Sriram, Ozluturk and Warty and further in view of U.S. Patent No. 6,161,024 to Komara (hereinafter "Komara").

The fourth issue is whether claims 20-24 are improperly finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Ozluturk in view of U.S. Patent Publication No. 2001/0034227 to Subramanian et al. (hereinafter "Subramanian").

ARGUMENT

Appellant respectfully requests the Board to reverse these grounds of rejection at least for the reasons set forth in the Appeal Brief filed on March 2, 2007 (hereinafter "Appeal Brief"). Furthermore, although Appellant believes that the Appeal Brief adequately addresses the Examiner's position, Appellant further addresses Examiner's position set forth in the Examiner's Answer mailed July 18, 2007 (hereinafter "Examiner's Answer") herein below.

I. Claims 1, 3, 6-13, and 19 are Patentable over Sriram in view of Ozluturk.

Claims 1, 3, 6-13, and 19 are improperly finally rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,366,606 to Sriram (hereinafter "Sriram") in view of U.S. Patent No. 6,366,607 to Ozluturk et al. (hereinafter "Ozluturk").

The Examiner addressed the arguments set forth in the Appeal Brief with respect to claim 1 on pages 8-10 of the Examiner's Answer. In particular, the Examiner raised four points: a) taking the broadest possible interpretation, any device that performs chip rate processing can be considered to perform symbol rate processing, b) combining the correlator co-processor and digital signal processor is an obvious engineering choice, c) carrier offset correction allegedly performed by Ozluturk's processing unit 67 or 157 discloses symbol processing and chip rate processing, and d) the reason to combine the references is to eliminate extra circuitry. These four points are addressed in greater detail herein below.

A. Point 1 - Chip Rate processing is not the same as Symbol processing

The Examiner contends that Sriram's correlation controller 40 of correlator co-processor performs chip rate processing and symbol processing, as set forth in claim 1, because symbols are comprised of chips (*see* pages 8-9 of the Examiner's Answer). Accordingly, the Examiner contends that "any device that performs chip rate processing can also be considered to perform symbol processing" (*see* page 9 of the Examiner's Answer). The Examiner further dismisses Sriram's "symbol processor 37" provided in a separate component, *i.e.,* a receiver 10, as allegedly disclosing <u>additional</u> symbol processing (*see* page 9 of the Examiner's Answer).

This position is inconsistent with the position advanced in the Office Actions, *e.g.*, see Final Office Action mailed July 5, 2006 ("Sriram fails to disclose that the symbol rate processing and chip rate processing are performed by a single processor," *see* page 2).

Furthermore, as noted in the previous responses, Sriram discloses a digital receiver 10, which is implemented on a DSP (col. 2, lines 31 to 33). The digital receiver 10 interfaces with a programmable correlator co-processor 12. The correlator co-processor is <u>not</u> positioned in the receiver but is a <u>separate unit</u> that communicates with the receiver. It is this correlator co-processor that performs the chip rate processing. The correlator co-processor performs chip rate processing using a chip correlator 34 (col. 2, lines 49 to 54; col. 3, lines 34 to 50). The DSP (the digital receiver) performs the symbol processing (Fig. 2; col. 5, lines 51 to 60). In other words, Sriram is no different from the prior art disclosed in the background of the invention; Sriram teaches a receiver 10 having a symbol processor 37 performing symbol processing and a co-

processor 12 performing a chip rate processing (Fig. 2; col. 3, lines 34 to 50 and col. 4, lines 28 to 42).

In addition, the Examiner's position that chip rate processing broadly discloses symbol processing since symbols are made of chips is inconsistent with the specification and their ordinary meaning in the art. Chip rate processing, as is known, relates to processing at the chip level *i.e.*, dispreading information based on users and symbol processing, as is known, relates to processing information at the symbol level *i.e.*, decoding received information.

See e.g., page 1, line 16 to page 2, line 2 of the specification, which describes that for the reception of the transmitted information, it is necessary to perform so-called chip rate processing and so-called symbol processing. The outlay for the chip rate processing is substantially dependent upon the number of existing users. The outlay for the symbol processing is substantially dependent upon the existing data rate. Furthermore, as is known, the chip rate processing is performed with the aid of so-called field programmable gate arrays (FPGAs) or Application Specific Integrated Circuits (ASICs), while normally so-called digital signal processors (DSPs) are used for the symbol processing. The number of the FPGAs and/or ASICs must be selected such that the chip rate processing can still be performed in the case of the maximum possible number of users. Correspondingly, the number of the DSPs must be selected such that the symbol processing can still be performed in the case of the maximum possible data rate. *Also see e.g.*, page 5, lines 21 to 31 of the specification.

A claim cannot be given an interpretation that is inconsistent with the ordinary meaning and the specification, MPEP § 2111.01. Accordingly, Appellant maintains that Sriram does not suggest "a digital processor that can perform both symbol rate processing and at least a portion of the chip rate processing," as recited in claim 1.

B. Point 2 - Combining the co-processor and digital processor is <u>not</u> an obvious Engineering Choice

The Examiner contends that combining the correlator co-processor and digital signal process is an obvious engineering choice, (*see* page 9 of the Examiner's Answer). Appellant respectfully submits that in *Schenck v. Nortron Corp.*, 713 F.2d 782, 218 USPQ 698 (Fed. Cir. 1983), claims were directed to a vibratory testing machine (a hard-bearing wheel balancer) comprising a holding structure, a base structure, and a supporting means which form "a single integral and gaplessly continuous piece." Nortron argued that the invention is just making integral what had been made in four bolted pieces. The court found this argument unpersuasive and held that the claims were patentable because <u>the prior art perceived a need for mechanisms to dampen resonance, whereas the inventor eliminated the need for dampening via the one-piece gapless support structure, showing insight that was contrary to the understandings and expectations of the art</u>, MPEP § 2144.04.

Similarly, as is known, in the prior art, each base stations should have a predetermined number of field programmable gate arrays (FPGAs) or Application Specific Integrated Circuits (ASICs) so that the FPGAs or ASICs will be able to accommodate maximum number of users. Similarly, the number of digital signal processors (DSP) is predetermined to support the

maximum possible data rate. However, the situation is such that there are either a maximum number of users with a low data rate or a small number of users with a maximum data rate. The maximum data rate and the maximum number of users can never be present at the same time however. This has the result that on the one hand, the base station must in each instance be equipped for the described maximum situations in respect of the number of FPGAs and ASICS and the number of DSPs, whereas on the other hand these maximum situations can never occur simultaneously. Consequently, either a part of the FPGAs or ASICS or a part of the DSPs is always unused, which is synonymous with an over-dimensioning of the base station in this respect (*see e.g.*, page 1, line 24 to page 2, line 14 of the specification). Just like in *Schenck v. Nortron Corp.*, an exemplary embodiment of the present invention eliminated the over dimensioning of the base station by having the processors perform chip rate processing or symbol processing, as needed (*see* page 2, lines 16 to 29 of the specification). An exemplary embodiment of the present invention shows insight that is contrary to the understandings and expectations of the art *e.g.*, background of the invention, Sriram (chip processor co-processor 12 and symbol rate processor receiver 10) and Ozluturk (despreaders are separate from decoders/signal processors).

In other words, Appellant respectfully submits that having a DSP that would perform both chip rate processing and symbol processing is not an obvious engineering choice. On the contrary, the implementation of chip rate processing on a DSP would have been <u>very inefficient</u> at the time the above-identified application was filed as the base operation for despreading and

spreading (complex multiplication of 1 bit by complex values of n bits) could have been implemented only very inefficiently on a DSP. Furthermore, ASIC or FPGA based solutions were much cheaper. Accordingly, a method of load balancing between symbol processing and chip rate processing by using special commands for a reasonable use of DSPs is not an obvious engineering choice.

Accordingly, the features of claim 1 are unobvious in view of the prior art of record.

C. Point 3 - Carrier Offset Correction of Ozluturk is not the chip rate processing and symbol rate processing set forth in claim 1

The Examiner contends that carrier offset correction allegedly performed by Ozluturk's processing unit 67 or 157 discloses both the symbol rate processing and chip rate processing (*see* pages 9-10 of the Examiner's Answer). Appellant respectfully submits that this point was addressed in the Appellant's Appeal Brief (*see* pages 18-22 of the Appeal Brief).

Appellant further respectfully submits that carrier offset correction is not chip rate or symbol processing, as explained above in Point 1. Appellant further respectfully submits that Ozluturk discloses performing the carrier-offset correction at chip level **or** symbol level. Ozluturk further notes the advantages and disadvantages of performing the corrections at each level (col. 4, lines 1 to 14). In short, Ozluturk does not cure the above-noted deficiencies of Sriram.

D. Point 4 - Reasons for the Combination are based on impermissible hindsight

The Examiner further contends that one of ordinary skill in the art would combine the reference to eliminate extra circuitry (*see* page 10 of the Examiner's Answer). Appellant

respectfully submits that the proposed combination is based on Appellant's disclosure, as addressed in the Appeal Brief (*see* page 17 of the Appeal Brief).

Furthermore, Appellant respectfully submits that the proposed combination is unworkable in that one of ordinary skill in the art would not replace chip rate processing and symbol processing as allegedly disclosed by Sriram with a correlator of Ozluturk. In other words, if the signal is not despread (chip rate processed), then correlation is useless. In short, but for the present invention, one of ordinary skill in the art would not have combined Ozluturk with Sriram as suggested by the Examiner. The proposed combination is a creature of impermissible hindsight.

In summary, Appellant respectfully submits that one of ordinary skill in the art would not have been motivated to combine the references in the manner suggested by the Examiner without exercising impermissible hindsight. Furthermore, the combined disclosures of Sriram and Ozluturk do not suggest the unique features of claims 1 and 9-12 discussed above. Ozluturk despreads the signals *i.e.*, performs the chip rate processing, prior to providing them to the processor, which only performs the symbol rate processing. For at least these exemplary reasons, claims 1 and 9-12 are patentable over Sriram in view of Ozluturk. Accordingly, Appellant respectfully requests the honorable Board to reverse this rejection of claims 1 and 9-12. Claims 3, 6-8, 13, and 19 are patentable at least by virtue of their dependency on claim 1 or 12.

<u>Issue 2: Claims 2, 14, and 16 are Patentable over Sriram and Ozluturk in view of Warty.</u>

Claims 2, 14, and 16 are improperly finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Sriram and Ozluturk in view of U.S. Patent No. 4,827,499 to Warty (hereinafter "Warty"). Since claims 2 depends on claim 1 and claims 14 and 16 depend on claim 12, they are patentable at least by virtue of their dependency, as set forth on pages 21-22 of the Appeal Brief.

<u>Issue 3: Claims 4, 5, and 15 are Patentable over Sriram Ozluturk, and Warty, in view of Komara.</u>

Claims 4, 5, and 15 are improperly finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Sriram, Ozluturk and Warty in view of U.S. Patent No. 6,161,024 to Komara (hereinafter "Komara"). Since claims 4 and 5 depend on claim 1 and claim 15 depends on claim 12, they are patentable at least by virtue of their dependency, as set forth on page 22 of the Appeal Brief.

In response to additional arguments regarding claim 5, (which recites "wherein the chip rate processing and the symbol processing can be distributed between sub-arrays or sub-groups of signal processors"), the Examiner contends that DSP <u>**may**</u> each process a number of digital channel signals at same time, relying on col. 4, lines 35 to 42 (*see* pages 10-11 of the Examiner's Answer). Col. 4, lines 35 to 42 of Komara recite:

> The demodulators 18-1 are each programmed to demodulate each channel signal 15 as specified by the air interface standard supported by the base station 10. <u>There typically is not a one-to-one correspondence between the number of DSP demodulators 18-1 and</u>

> <u>the number of channel signals</u>, n, provided by the channelizers 14 in each transceiver 31-34. For example, the DSP's may each process a number, such as 24, of digital channel signals 15 at the same time.

In other words, Komara simply discloses that the correspondence of the DSPs and digital channel signals are not one to one and <u>not</u> that the chip rate processing <u>**and**</u> the symbol processing is distributed between sub-arrays or sub-groups of signal processors. That is, Komara does not disclose that DSPs are not split into groups such that one group performs chip rate processing and another group performs symbol processing but only discloses that one group modulates the signal and another group demodulates the signal (col. 2, line 54 to col. 3, line 10). In short, Sriram, Ozluturk, Warty, and Komara, taken alone or in any conceivable combination, fail to disclose or suggest the unique features of claim 5. For at least these additional exemplary reasons, claim 5 is patentable over the prior art of record.

<u>**Issue 4: Claims 20-24 are Patentable over Ozluturk in view of Subramanian**</u>

Claims 20-24 are improperly finally rejected under 35 U.S.C. § 103(a) as being unpatentable over Ozluturk in view of U.S. Publication No. 2001/0034227 to Subramanian et al. (hereinafter "Subramanian"). Appellant respectfully maintains all arguments with respect to these claims as set forth in the Appeal Brief on pages 23-29.

In addition, Appellant respectfully notes that claims 22 and 23 <u>cannot be obvious over Ozluturk and Subramanian and this rejection is improper</u>. Claims 22 and 23 depend on claim 1 and as such contain all the features of independent claim 1. <u>The Examiner has not shown how the combined disclosure of Ozluturk and Subramanian meet the unique features of claim 1.</u>

Appellant respectfully submits that the combined disclosures of Ozluturk and Subramanian do not meet all of the unique features of claim 1. Accordingly, claims 22 and 23 cannot be obvious over Ozluturk in view of Subramanian at least by virtue of their dependency. This deficiency has not been addressed in the Examiner's Answer.

Appellant further respectfully notes that Subramanian relates to a method of generating a configuration for a configurable spread spectrum communication device. That is, Subramanian discloses a complex computing device which generates a signal flow path and maps it onto various configurable elements of the configurable device. This computing device needs its own processor, memory and user interface (*see* Abstract and ¶¶ 9 through 11). In other words, Subramanian does not disclose or suggest having a single processor perform the chip rate processing, the symbol rate processing, and the switching. In Subramanian, a separate computing device with a memory and a user interface is provided to map out the signal flow (element 102 in Fig. 1A and Fig. 2; ¶¶ 21 and 30). Then, the mapped out signal flow is transferred to the configurable device 104 for implementation (Fig. 1; ¶¶ 22 and 24). In other words, Subramanian clearly discloses separate devices for the spread spectrum processing and for the switching. Subramanian does not cure the deficient disclosure of Ozluturk.

The Examiner contends that an external computing device 102 of Subramanian can be placed into the processor of Ozluturk (*see* page 12 of the Examiner's Answer). Appellant respectfully submits that the proposed combination is unworkable. As is known, a digital signal

processor is a microprocessor that would not include a user interface and an interface to communicate to another remote computing device, as disclosed in Subramanian (¶¶ 21 to 23).

Furthermore, it is respectfully submitted that Examiner is clearly exercising impermissible hindsight. Specifically, the Examiner contends that one of ordinary skill in the art would have combined the references "to perform the most effective processing based on the type of processing required at any given time" (*see* page 12 of the Examiner's Answer). Appellant respectfully notes that the claims are not directed to *any* processing sharing resources but rather the chip rate processing sharing a digital signal processor that performs the symbol processing when conventionally the chip rate processing would be implemented by different physical devices (FPGA or ASIC vs. DSP). In other words, it is the claimed invention that discloses an effective way of performing the chip rate processing and the symbol processing by sharing DSP and none of the prior art references of record disclose these unique features. On the contrary, in the prior art, it is known that the implementation of chip rate processing on a DSP would be very inefficient as the base operation for despreading and spreading (complex multiplication of 1 bit by complex values of n bits) could be implemented only very inefficiently on a DSP and very expensive as ASIC and FPGA are cheaper.

In short, one of ordinary skill in the art would not have combined the references in the manner suggested by the Examiner.

CONCLUSION

For the above reasons as well as the reasons set forth in Appeal Brief, Appellant respectfully requests that the Board reverse the Examiner's rejections of all claims on Appeal. A favorable decision on the merits of this Appeal is respectfully requested.

Respectfully submitted,

/Nataliya Dvorson/
Nataliya Dvorson
Registration No. 56,616

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
23373
CUSTOMER NUMBER

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